"PVCNSSK" GOVT. POLYTECHNIC BILASPUR at KALOL

PLANNED THEORY SYLLABUS COVERAGE

PTSC-7.1

GPB	Department: Electrical Engg.	Subject: Digital Electronics	
	Sem. & Branch : 4th & EE	Duration : 3years	

| SYLLABUS COVERAGE | Total Periods: Theory:56   Practical:28 | | |

Sr No	Period Nos	Topic	Details	Instruction Reference	Additional Study Recommended	Remarks
1	5(1-5)	Introduction	Analog Signal, Digital Signal, Difference between Analog & Digital Signal, Applications & Advantages of Digital Signal.			
2	7(6-12)	Number System	- Binary, Octal, & Hexadecimal number systems, Conversion from Decimal, Octal & Hexadecimal Systems to Binary System & Vice Versa. - Binary Addition, Subtraction, Multiplication, Division, 1's and 2's compliment methods of subtraction, Concept of code: 8421, BCD, Excess 3 and Gray Code, Concept of Parity.			
3	9(13-21)	Logic Gates & Families	- Logic symbol, logical expression and truth table of AND, OR, NOT, NAND, NOR, EX- OR gates, -Universal property of NAND and NOR gate. - Logic Simplification Circuits-Basic laws of Boolean algebra, Duality theorem, De Morgan's Theorems. - Boolean expressions using Sum of Products (SOP) and Product of Sums (POS) forms. - K-map representation of logical functions. - Minimization of logical expressions using K-map (2, 3, 4 variables). -Logic Gates & Families (SSI, MSI, LSI, VLSI, ULSI)			

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5	7(22-28)	Arithmetic Circuits	- Half Adder/Full Adder Circuit, their design and implementation, Half Subtracter /Full Subtracter Circuit, their design and implementation.			
6	8(29-36)	Decoder, Encoder, Multiplexer & De-Multiplexer	- Basic binary decoder, Encoder-Decimal to BCD Encoder - Block diagram, Truth table, Logical expression and logic diagram of Multiplexers (4:1 and 8:1). - Block diagram and Truth table of Demultiplexer (1:4 and 1:8)			
7	12(37-48)	Flip Flops, Counters, Shift-Registers	-One-bit memory cell, clock signal, Latch-SR Latch, Difference between Latch & Flip-Flop -**Flip Flops**: S-R Flip flop, D- Flip Flop, J-K Flip Flop, Master Slave Flip-Flop, T- Flip Flop -**Counters:** Asynchronous Counters/Ripple Counter (2 bit, 3-bit, Decade) : Synchronous Counters (2-bit, 3-bit, decade synchronous counter), Ring Counter **Shift Registers:** Concept of Shift registers, Types of Shift registers (SISO, SIPO, PISO, PIPO and Universal Shift Registers) - Applications of Flip-Flops, Counters & Shift Registers			
8	3(49-51)	Memories 03 hrs	Classification of Memories RAM, ROM, PROM, EPROM, E2PROM, Cache Memory, Static and Dynamic RAM			
9	5(52-56)	D/A & A/D Converters	- Digital to Analog Converters (Weighted register, R-2R Ladder D/A Converter) -Analog to Digital Converter (Dual Slope method, Successive Approximation A/D Converter) - Applications of A/D & D/A Converter			

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DATE ---13/07/22---	
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